WHAT IS CLAIMED IS:

1. A programmable logic integrated circuit comprising:

a programmable logic portion; and

an embedded processor portion coupled to the programmable logic portion and comprising:

a processor; and

a memory block coupled to the processor and comprising:

a memory having a first port and a second port; and

an arbiter coupled to the first port and the second port, wherein the arbiter arbitrates access to the memory by the first port and the second port.

2. The integrated circuit of claim 1 wherein the memory is a dual-port SRAM.

3. The integrated circuit of claim 2 wherein the programmable logic portion comprises a plurality of logic elements, programmably configurable to implement user-defined combinatorial or registered logic functions.

4. The integrated circuit of claim 3 wherein the programmable logic portion further comprises a plurality of horizontal and vertical interconnect lines, programmably coupled to the plurality of logic elements.

5. The integrated circuit of claim 1 wherein the second port is configurable in width and depth.

6. The integrated circuit of claim 1 wherein the first port and the second port are both configurable in width and depth.

7. A programmable logic integrated circuit comprising:

a programmable logic portion comprising a plurality of logic elements, programmably configurable to implement user-defined combinatorial or registered logic functions; and

an embedded processor portion coupled to the programmable logic portion and comprising:

a processor; and

a memory block coupled to the processor and comprising:

a first plurality of memory cells for storing data;

a second plurality of memory cells for storing data;

a first port coupled to the first and second pluralities of memory cells;

a second port coupled to the first and second pluralities of memory cells; and

an arbiter coupled to the first port and the second port,

wherein when the second port is accessing the first plurality of memory cells, the arbiter prevents the first port from accessing the first plurality of memory cells, and when the second port is accessing the first plurality of memory cells, the arbiter allows the first port to access the second plurality of memory cells.

8. The integrated circuit of claim 7 wherein the first plurality of memory cells and the second plurality of memory cells are defined by a user-programmable lock register.

9. The integrated circuit of claim 8 wherein the first and second pluralities of memory cells comprise a portion of a dual-port SRAM.

10. The integrated circuit of claim 9 wherein the programmable logic portion further comprises a plurality of horizontal and vertical interconnect lines, programmably coupled to the plurality of logic elements.

11. The integrated circuit of claim 10 wherein the second port is configurable in width and depth.

12. The integrated circuit of claim 10 wherein the first port and the second port are both configurable in width and depth.

13. A method of arbitration in a programmable logic integrated circuit comprising a programmable logic portion coupled to an embedded processor portion, the

embedded processor portion comprising a memory having a first port and a second port, the first port and the second port coupled to an arbiter, the method comprising:

sending a lock request from the second port to the arbiter when the second port requires access to the memory;

sending a lock grant from the arbiter to the second port if the first port is not accessing the memory; and

not sending a lock grant from the arbiter to the second port if the first port is accessing the memory.

14. The method of claim 13 further comprising:

when sending a lock grant from the arbiter to the second port, sending a wait state from the arbiter to the first port.

15. The method of claim 13 further comprising:

when sending a lock grant from the arbiter to the second port, writing data from the second port to the memory;

de-asserting the lock request from the second port to the arbiter; and

de-asserting the lock grant from the arbiter to the second port.

16. The method of claim 13 further comprising:

when sending a lock grant from the arbiter to the second port, reading data from the memory to the second port;

de-asserting the lock request from the second port to the arbiter; and

de-asserting the lock grant from the arbiter to the second port.

17. A method of arbitration in a programmable logic integrated circuit comprising a programmable logic portion coupled to an embedded processor portion, the embedded processor portion comprising a memory coupled to an arbiter, wherein the memory comprises a plurality of memory cells, a first port coupled to the plurality of memory cells, and a second port coupled to the plurality of memory cells, the method comprising:

storing a value in a lock register, wherein the value defines a first portion of memory cells and a second portion of memory cells within the plurality of memory cells,

wherein the arbiter arbitrates access to the first portion of memory cells by the second port, and does not arbitrate access to the second portion of memory cells by the second port.

18. The method of claim 17 further comprising:

providing an address of a memory location at the first port;

determining if the memory location is in the second portion of memory cells, and if it is; then

allowing access of the memory by the first port.

19. The method of claim 17 further comprising:

determining whether a transfer at the second port is to the first portion of memory cells, and if it is; then

sending a lock request from the second port to the arbiter.

20. The method of claim 17 further comprising:

providing an address of a memory location at the first port;

determining if the memory location is in the first portion of memory cells; and if it is, then

determining whether the second port has been granted a lock to the first portion of memory cells; and if it has, then

waiting until the second port is not granted a lock to the first plurality of memory cells; else

transferring data at the first port.

21. The method of claim 17 further comprising:

determining whether a transfer at the second port is to the first portion of memory cells, and if it is; then

determining whether the first port is accessing the first portion of memory cells; and if it is, then waiting until the first port is not accessing the first portion of memory cells; else

transferring data at the second port.

22. A method of laying out a programmable logic device having an embedded processor comprising:

providing a layout of a programmable logic device, the programmable logic device having four sides;

stretching one side of the programmable logic device, such that an open space is created; and

placing the layout of an embedded processor in the open space,

wherein the embedded processor comprises a memory having a first port and a second port, and an arbiter coupled to the first port and the second port.

23. The method of claim 22 wherein the embedded processor further comprises a first bus coupled to the processor and the first port, and a second bus coupled to the first port.

24. The method of claim 23 further comprising coupling signal lines between the layout of the programmable logic device and the layout of the embedded processor.

25. A method of laying out a programmable logic device having an embedded processor comprising:

providing a layout of a programmable logic device, the programmable logic device having four sides;

stretching one side of the programmable logic device, such that an open portion of the layout is created; and

laying out an embedded processor in the open portion of the layout,

wherein the embedded processor comprises a dual port memory and an arbiter, wherein the arbiter arbitrates access to the dual port memory.

26. The method of claim 25 wherein the embedded processor comprises a dual-port SRAM.

27. The method of claim 26 further comprising coupling signal lines between the layout of the programmable logic device and the layout of the embedded processor.

28. A programmable logic integrated circuit comprising:

a programmable logic portion comprising a plurality of logic elements, programmably configurable to implement user-defined combinatorial or registered logic functions; and

an embedded processor portion coupled to the programmable logic portion and comprising:

a processor;

a first bus coupled to the processor;

a memory coupled to the first bus and the programmable logic portion; and

a second bus coupled to the memory.

29. The integrated circuit of claim 28 wherein the memory is a dual-port SRAM.

30. The integrated circuit of claim 28 wherein the memory further comprises a first port and a second port, and the embedded processor further comprises:

a multiplexer having a first input coupled to the first bus, a second input coupled to the second bus, and an output coupled to the first port.

31. The integrated circuit of claim 30 wherein the embedded processor further comprises an arbiter coupled to the multiplexer and the second port,

wherein the arbiter arbitrates access to the memory by the first bus, the second bus, and the second port.

32. A programmable logic integrated circuit comprising:

a programmable logic portion comprising a plurality of logic elements, programmably configurable to implement user-defined combinatorial or registered logic functions; and

an embedded processor portion coupled to the programmable logic portion and comprising:

a plurality of memory cells;

a first port coupled to the plurality of memory cells;

a second port coupled to the plurality of memory cells;

a multiplexer coupled to the first port;

an arbiter coupled to the first port, the second port, and the multiplexer; and

a lock register to store a user-defined variable lock size and coupled to the arbiter,

wherein the user-defined variable lock size defines a lockable portion of the plurality of memory cells and a non-lockable portion of the plurality of memory cells, and wherein the arbiter arbitrates access by the second port to the lockable portion of the plurality of memory cells, and does not arbitrate access by the second port to the non-lockable portion of the plurality of memory cells.

33. The integrated circuit of claim 32 the embedded processor portion further comprises:

a first bus coupled to the multiplexer;

a second bus coupled to the multiplexer; and

a processor coupled to the first bus.

34. The integrated circuit of claim 32 wherein when the second port requires access to the lockable portion of the memory, the second port sends a lock request to the arbiter, the arbiter determines whether the first port is accessing the lockable portion of the memory, the arbiter sends a lock grant signal to the second port if the first port is not accessing the lockable portion of the memory, and the arbiter does not send the lock grant signal if the first port is accessing the lockable portion of the memory, and wherein when the second port requires access to the non-lockable portion of the memory, it accesses the non-lockable portion of the memory without sending the lock request to the arbiter.

35. The integrated circuit of claim 32 wherein when the first bus requires access to the memory, the first bus sends a request to the arbiter, the arbiter determines whether the second bus has access to the memory, the arbiter determines whether the first bus requires access to the lockable portion of the memory if the second bus does not have access to the

memory, and the arbiter determines if the second port has been granted a lock to the lockable portion of the memory if the first bus requires access to the lockable portion of the memory.

36. An embedded processor comprising:

a plurality of memory cells;

a first port coupled to the plurality of memory cells;

a second port coupled to the plurality of memory cells;

a multiplexer coupled to the first port;

a first bus coupled to the multiplexer;

a second bus coupled to the multiplexer; and

a processor coupled to the first bus.

37. The embedded processor of claim 36 wherein the embedded processor is integrated in a programmable logic integrated circuit.

38. A programmable logic integrated circuit comprising:

a programmable logic portion; and

an embedded processor portion coupled to the programmable logic portion and comprising:

a processor; and

a memory coupled to the processor and comprising:

a plurality of memory cells;

a first port coupled to the plurality of memory cells; and

a second port coupled to the plurality of memory cells and the programmable logic portion,

wherein the second port has a configurable width and a configurable depth, and wherein when the width of the second port is decreased, a depth of a memory map is increased and a width of the memory map is not changed, and when the width of the second port is increased, the depth of the memory map is decreased and the width of the memory map is not changed.

39. The integrated circuit of claim 38 wherein when the width of the second port is increased, the depth is decreased, and when the width of the second port is decreased, the depth is increased.

40. The integrated circuit of claim 39 wherein the first port has a configurable width and a configurable depth, and when the width of the first port is increased, the depth is decreased, and when the width of the first port is decreased, the depth is increased.

41. The integrated circuit of claim 40 further comprising an arbiter, wherein the arbiter arbitrates access to the memory cells by the first port and the second port.

42. A programmable logic integrated circuit comprising:

a programmable logic portion; and

an embedded processor portion coupled to the programmable logic portion and comprising:

a first number of lockable memory cells;

a second number of non-lockable memory cells;

a first port coupled to the lockable and non-lockable memory cells;

a second port coupled to the lockable and non-lockable memory cells and the programmable logic portion;

an arbiter coupled to the first port and the second port; and

a variable lock size register coupled to the arbiter, wherein the register stores a user-programmable lock size value,

wherein the first number and the second number equal a third number, and the first number and second number are variable and determined by the user-programmable lock size value, the third number is not variable, and wherein the arbiter arbitrates access to the lockable memory cells by the second port, and does not arbitrate access to the non-lockable memory cells by the second port.

43. The integrated circuit of claim 42 wherein the embedded processor portion further comprises:

a multiplexer coupled to the arbiter and the first port;

a first bus coupled to the multiplexer;

a second bus coupled to the multiplexer; and

a processor coupled to the first bus.

44. A programmable logic integrated circuit comprising:

a programmable logic portion; and

an embedded processor portion coupled to the programmable logic portion and comprising:

a first memory having a first and second port, the second port configured to have a first width and a first depth;

a second memory having a third and fourth port, the fourth port configured to have the first width and the first depth; and

a deep/wide multiplexing circuit coupled to the second port, the fourth port, and the programmable logic portion,

wherein the deep/wide multiplexing circuit multiplexes signals to and from the programmable logic portion such that the second and fourth ports appear to the programmable logic portion as one port with either a second width twice the first width, or a second depth twice the first depth.

45. The integrated circuit of claim 44 wherein when the second and fourth ports appear to the programmable logic portion as one port with a width twice the first width, the depth is the first depth, and when the second and fourth ports appear to the programmable logic portion as one port with a depth twice the first depth, the width is the first width.